

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1 1. (Currently Amended) A method to polish down conductive lines in the
2 manufacture of an integrated circuit device, said method comprising:
3 providing a plurality of conductive lines overlying a substrate;
4 depositing a high density plasma (HDP) oxide layer overlying said substrate and
5 said conductive lines wherein, in the regions between said conductive lines, first planar
6 surfaces of said HDP oxide layer are formed below the top of said conductive lines;
7 depositing a polish stopping layer overlying said HDP oxide layer;
8 depositing a film layer overlying said polish stopping layer;
9 polishing down said film layer to said polish stopping layer overlying said
10 conductive lines ~~second planar top surfaces~~; and
11 polishing down said film layer, said polish stopping layer, said HDP oxide layer
12 and said conductive lines to portions of said polish stopping layer overlying said first
13 planar top surfaces to complete said polishing down of said conductive lines.

1 2. (Cancelled)

1 3. (Original) The method according to Claim 1 wherein said conductive lines
2 comprise polysilicon lines.

1 4. (Currently Amended) The method according to Claim 1 wherein said
2 conductive lines comprise n-type polysilicon and further comprising the steps of:
3 forming an oxide layer overlying said conductive lines after said step of polishing
4 down said film layer, said ~~polish~~ polishing stop layer, said HDP oxide layer and said
5 conductive lines;
6 depositing a p-type polysilicon layer overlying said oxide layer; and
7 patterning ~~patterning~~ said p-type polysilicon layer to form p type polysilicon lines
8 that cross over said conductive lines with said oxide layer therebetween.

1 5. (Original) The method according to Claim 4 wherein said conductive lines are
2 bit lines and said p-type polysilicon lines are word lines for a non-volatile memory
3 device.

1 6. (Original) The method according to Claim 5 wherein other said conductive
2 lines are not bit lines but are used to provide a uniform pattern density of said
3 conductive lines across said substrate.

1 7. (Original) The method according to Claim [[1]] 42 wherein said step of
2 sputtering down said HDP oxide layer comprises bombardment with argon ions.

1 8. (Original) The method according to Claim 1 wherein said film layer comprises
2 silicon oxide and said polish stopping layer comprises silicon nitride.

1 9. (Original) The method according to Claim 8 wherein said film layer comprises
2 high density plasma (HDP) oxide.

1 10. (Original) The method according to Claim 8 wherein said film layer
2 comprises chemical vapor deposited (CVD) oxide.

1 11. (Currently Amended) A method to polish down polysilicon lines in the
2 manufacture of an integrated circuit device, said method comprising
3 providing a plurality of polysilicon lines overlying a substrate.

4 ~~Depositing~~ depositing a high density plasma (HDP) oxide layer overlying said
5 substrate and said polysilicon lines wherein, in the regions between said polysilicon
6 lines, first planar top surfaces of said HDP oxide layer are formed below the top of said
7 polysilicon lines;

8 sputtering down said HDP oxide layer overlying said polysilicon lines such that
9 second planar top surfaces of said HDP oxide layer are formed above said polysilicon
10 lines;

11 thereafter depositing a polish stopping layer overlying said HDP oxide layer;

12 depositing a film layer overlying said polish stopping layer;

13 polishing down said film layer to said polish stopping layer overlying said second
14 planar top surfaces; and
15 polishing down said film layer, said polish stopping layer, said HDP oxide layer
16 and said polysilicon lines to said polish stopping layer overlying said first planar top
17 surfaces to complete said polishing down of said polysilicon lines.

1 12. (Original) The method according to Claim 11 wherein said polysilicon lines
2 comprise n-type polysilicon and further comprising the steps of
3 forming an oxide layer overlying said polysilicon lines after said step of polishing
4 down said film layer, said polishing stop layer, and said polysilicon lines;
5 depositing a p-type polysilicon layer overlying said oxide layer; and
6 patterning said p-type polysilicon layer to form p type polysilicon lines that cross
7 over said n-type polysilicon lines with said oxide layer therebetween.

8 13. (Original) The method according to Claim 12 wherein said n-type polysilicon
9 lines are bit lines and said p-type polysilicon lines are word lines for a non-volatile
10 memory device.

1 14. (Original) The method according to Claim 13 wherein other said n-type
2 polysilicon lines are not bit lines but are used to provide a uniform pattern density of
3 said polysilicon lines across said substrate.

1 15. (Original) The method according to Claim 11 wherein said polysilicon lines
2 further comprise a stack of a second polysilicon layer overlying a first polysilicon layer
3 with a metal silicide layer therebetween

1 16. (Original) The method according to Claim 11 wherein said step of sputtering
2 down said HDP oxide layer comprises bombardment with argon ions.

1 17. (Original) The method according to Claim 11 wherein said film layer
2 comprises silicon oxide and said polish stopping layer comprises silicon nitride.

1 18. (Original) The method according to Claim 17 wherein said film layer is high
2 density plasma (HDP) oxide CVD oxide.

1 19. (Currently Amended) A method to form anti-fuse memory devices in the
2 manufacture of an integrated circuit device, said method comprising
3 providing a plurality of n-type polysilicon lines overlying a substrate;
4 depositing a high density plasma (HDP) oxide layer overlying said substrate and
5 said n-type polysilicon lines wherein, in the regions between said n-type polysilicon
6 lines, first planar top surfaces of said HDP oxide layer are formed below the top of said
7 n-type polysilicon lines;
8 sputtering down said HDP oxide layer overlying said n-type polysilicon lines such
9 that second planar top surfaces of said HDP oxide layer are formed above said n-type
10 polysilicon lines;
11 thereafter depositing a polish stopping layer overlying said HDP oxide layer;
12 depositing a film layer overlying said polish stopping layer;
13 polishing down said film layer to said polish stopping layer overlying said second
14 planar top surfaces;
15 polishing down said film layer, said polish stopping layer, said HDP oxide layer
16 and said n-type polysilicon lines to said polish stopping layer overlying said first planar
17 top surfaces to complete said polishing down of said n-type polysilicon lines;
18 forming a dielectric layer overlying said n-type polysilicon lines;
19 depositing a p-type polysilicon layer overlying said dielectric layer; and
20 patterning said p-type polysilicon layer to form p-type polysilicon lines that cross
21 over said n-type polysilicon lines with said oxide layer therebetween to thereby
22 complete said anti-fuse memory devices.

1 20. (Original) The method according to Claim 19 wherein said n-type polysilicon
2 lines are bit lines and said p-type polysilicon lines are word lines for a non-volatile
3 memory device. ++

1 21. (Original) The method according to Claim 19 wherein other said n-type
2 polysilicon lines are not bit lines but are used to provide a uniform pattern density of
3 said n-type polysilicon lines across said substrate.

1 22. (Currently Amended) The method according to Claim 19 wherein said n-
2 type polysilicon lines further comprise a stack of a second polysilicon layer overlying a
3 first polysilicon layer with a metal silicide layer therebetween.

1 23. (Original) The method according to Claim 19 wherein said step of sputtering
2 down said HDP oxide layer comprises bombardment with argon ions.

1 24. (Original) The method according to Claim 19 wherein said dielectric layer
2 comprises silicon oxide or silicon nitride.

1 25. (Original) The method according to Claim 19 wherein said film layer
2 comprises silicon oxide and said polish stopping layer comprises silicon nitride.

1 26. (Original) The method according to Claim 25 wherein said film layer
2 comprises high density plasma (HDP) oxide.

1 27. (Original) The method according to Claim 25 wherein said film layer
2 comprises chemical vapor deposited (CVD) oxide.

1 Claims 28 to 41 (Cancelled).

1 42. (Previously Pending) The method as claimed in claim 1, further comprising
2 a step of sputtering down said HDP oxide layer overlying said conductive lines before
3 depositing the polish stopping layer such that second planar surfaces of said HDP oxide
4 layer are formed above said conductive lines.